30. The computer-readable medium of claim 29 further comprising a routing tool to route wires between the plurality of logic gates in the layout.

31. [Amended] A computerized system comprising:

a computer-readable medium;

a processor; and

a computer-aided design program stored on the computer-readable medium and executable by the processor, the computer-aided design program comprising a placement module to generate a layout of an integrated [intregrated] circuit wherein the placement module performs a reliability verification of the layout for self heat and electromigration considerations.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 25, 2001, and the references cited therewith.

Claims 1, 2, 7, 8, 22, 26, 29 and 31 are amended, claims 3, 9, 24 and 28 are canceled, and no claims are added; as a result, claims 1-2, 4-8, 10-23, 25-27, and 29-31 are now pending in this application.

Rejections Under 35 U.S.C.§102

Claims 1-4, 6-17, and 22-31 were rejected under 35 U.S.C.§102(b) as being anticipated by Ito (U.S. Patent No. 5,648,910).

Claims 1-4, 6-17, and 22-31 were rejected under 35 U.S.C.§102(b) as being anticipated by Hathaway et al. (U.S. Patent No. 5,737,580).

Appellant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation for the following reasons. Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). Amended independent claims 1, 7, 22, 26, 29 and 31 recites layout rules based on a reliability verification constraints arising from *self heat*.

In contrast, Ito describes "regulating the width of each power supply line incorporated in the power supply network on the basis of the amount of current passing therethrough so that the power supply network is free from electromigration." (see Abstract of Ito). However, Ito does not teach each elements of amended independent claims 1, 7, 22, 26, 29 and 31 which include layout rules based on a reliability verification constraints arising from *self heat.*

Furthermore, Hathaway describes "a technique to optimize the width of automatically routed wire segments so that these widths are adequate to support the electromigration current on the net as a function of the capacitive loading of the net itself" (see Abstract of Hathaway). However, Hathaway does not teach each elements of amended independent claims 1, 7, 22, 26, 29 and 31 which include layout rules based on a reliability verification constraints arising from *self heat.*

In addition, neither Ito or Hathaway describe minimizing a cost function having a reliability verification factor as claimed in independent claim 13.

1-4, 6-17, and 22-31

Claims 2-4, 6, 8-12, 14-17, 23-25, 27-28, and 30 depend, directly or indirectly, on claims 1, 7, 13, 22, 26, 29 and 31, respectively, and are patentable over Ito and Hathaway for the reasons argued above, plus the elements in the claims.

Rejections Under 35 U.S.C.§103

Claim 5 was rejected under 35 U.S.C.§103(a) as being unpatentable over Ito (U.S. Patent No. 5,648,910).

Claim 5 was rejected under 35 U.S.C.§103(a) as being unpatentable over Hathaway et al. (U.S. Patent No. 5,737,580).

Claims 18-21 were rejected under 35 U.S.C.§103(a) as being unpatentable over Hathaway et al. (U.S. Patent No. 5,737,580), in view of Gupta et al., *Optimal 2-D Cell Layout with Integrated Transistor Folding*, 1998 IEEE/ACM International Conference on Computer-Aided Design, 8 November 1998, pgs. 128-135.

The Examiner rejected claim 5 based on Ito individually and on Hathaway individually. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found either Ito or Hathaway individually. Since all the

elements of the claim are not found in the reference, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of Official Notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 706.02(a), Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

Claims 18-21 depend, directly or indirectly, on claim 13, respectively, and are patentable over Ito and Hathaway for the reasons argued above, plus the elements in the claims. If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. MPEP § 2143.03.

Conclusion

Applicant respectfully requests reconsideration and submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 26 day of March, 2002.

Jane E. Brockschink
Name

Signature